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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,421	04/13/2004	Daniel C. Guterman	SAND-01014US0	4027

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EXAMINER	
LE, TOAN K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/823,421	GUTERMAN, DANIEL C.
	Examiner	Art Unit
	Toan Le	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8,11-16,18,22-37,39 and 43-55* is/are rejected.

7)☒ Claim(s) *4-7,9,10,17,19-21,38 and 40-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/02/04; 8/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history*.

DETAILED ACTION

Information Disclosure Statement

1. This office acknowledge receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on August 12, 2005.

Information Disclosure Statement (IDS) filed on November 02, 2004.

2. Information disclosed and list on PTO 1449 was considered.

Drawings

3. Figures 1-4 should be designated by a legend such as **--Prior Art--** because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. Claim 26 is objected to because of the following informalities:

In claim 26, line 2: "a second group" will be understood as --said second group--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 8, 11-16, 18, 22-37, 39 and 43-55 are rejected under 35 U.S.C. 102(e) as being anticipated by Lutze et al. (US. 6,859,397).

The applied reference has a common **assignee** with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Lutze et al. disclose in Figs. 14-18, a method of programming non-volatile memory comprising: boosting a voltage potential of a channel of a first group (unselected word lines on the drain side and source side including word line on the source neighbor) of non-volatile storage elements (see figs. 14-18 and col. 12, lines 17-27); trapping at least a portion of said voltage potential in a portion of the channel associated with a first subset (unselected word lines on the source side) of said first group of non-volatile storage elements (see figs. 14-18 and col. 12, lines 17-27); and

enabling programming (applying a program voltage Vpgm) of a second group (the selected word line) of non-volatile storage elements subsequent to said step of trapping (see figs 14-18).

Regarding claims 2, 8, Lutze et al. disclose the step of boosting including applying a first boosting voltage (Vssb) to the first subset (unselected word lines on the source side) of the first group of non-volatile storage elements (see figs. 14-18) and applying a second boosting voltage (Vssb) to a second subset (the word line for source side neighbor) of the first group (see figs. 14, 16) wherein the second subset includes storage elements that are not included in the first subset (see fig. 16).

Regarding claim 3, Lutze et al. disclose in fig. 16, lowering (at t_i) the second boosting voltage (Vssb) prior to enabling programming (at t_1) to the second group (the selected word line) and being subsequent to the step of trapping (see fig. 16 and col. 13, lines 2-20).

Regarding claim 11, Lutze et al. disclose in figs. 14-18, the step of boosting including coupling the voltage potential onto the channel by applying the first boosting voltage and the second boosting voltage.

Regarding claims 12 and 13, Lutze et al. disclose inhibiting programming of said first group (unselected word line) of non-volatile storage elements during at least a portion of said step of boosting (see col. 11, lines 60-65) including applying a program inhibit voltage to a bit line of the first group (see col. 4. lines 5-7); and inhibiting programming of the second group (selected word line) of non-volatile storage elements during at least a portion of said step of boosting (see col. 11, line 65 to line 6 of col. 12)

including applying a program inhibit voltage to a bit line of the second group (see col. 4. lines 5-7).

Regarding claims 14-16, Lutze et al. disclose in fig. 16, the step of trapping includes lowering a boosting voltage applied to at least one non-volatile storage element that bounds said first subset of non-volatile storage elements wherein the at least one non-volatile storage element is part of the first subset of the first group or part of a second subset of the first group.

Regarding claims 18, 28 and 29, Lutze et al. disclose the first group of non-volatile storage elements being a first string of NAND flash storage elements; said second group of non-volatile storage elements being a second string of NAND flash storage elements; the first subset of the first group including a storage element to be inhibited; the second group including a storage element to be programmed; said storage element to be inhibited and said storage element to be programmed being both coupled to a first word line; and the step of boosting including applying at least one boosting voltage to the first group and the second group while inhibiting programming to the first group and the second group (see col. 5, lines 7-53).

Regarding claims 22-25, Lutze et al. disclose the first subset (unselected word lines on the source side) of the first group having a storage element to be inhibited, wherein the first subset further includes a source side non-volatile storage element adjacent to the storage element to be inhibited or a drain side non-volatile storage element adjacent to the storage element to be inhibited or two source side non-volatile storage elements adjacent to the storage element to be inhibited and two drain side non-volatile storage elements adjacent to the storage element to be inhibited (see fig. 6).

Regarding claims 26-27, Lutze et al. disclose the step of enabling programming to the second group including applying a program enable voltage (ground or zero volts) to a bit line of the second group (see col. 4, lines 4-6).

Regarding claims 30-32, Lutze et al. disclose the first group and the second group being part of an array of non-volatile storage elements (see fig. 6); the array being in communication with a host system; the array being removable from said host system or embedded in the host system (see col. 6, line 65 to line 12 of col. 7); and the first group and second group being groups of multi-state non-volatile storage elements (see fig. 12).

Regarding claims 33 and 48, Lutze et al. disclose a non-volatile memory system comprising: a first group of non-volatile storage elements including a first and second subset (unselected word lines on the drain side and source side including word line on the source neighbor) of non-volatile storage elements (see Figs. 6 and 14-18), the first subset (the word line for the source side neighbor) of the first group including a non-volatile storage element to be inhibited; a second group (the selected word line) of non-volatile storage elements including a third and fourth subset of non-volatile storage elements (see fig. 6), the third subset of the second group including a non-volatile storage element to be programmed (the cell on the selected word line); and a plurality of word lines coupled to said first group and said second group (see fig. 6) to apply one or more boosting voltages to raise a voltage potential of a channel of said first group (see col. 5, lines 24- 28) wherein the plurality of word lines includes a first word line coupled to said storage element to be inhibited and to said storage element to be programmed (see col. 5, lines 19-22 and lines 46-48), the first word line applies a program voltage to said storage element to be programmed during a program operation (see col. 5, lines 46-49), the

plurality of word lines includes at least one bounding word line (the word line source side neighbor)having said boosting voltage lowered thereon, prior to applying said program voltage on said first word line, in order to trap said voltage potential in a portion of said channel associated with said first subset of said first group (see figs. 6 and 16).

Regarding claims 34-37, Lutze et al. disclose the plurality of word lines including a first plurality of word lines coupled to the first subset of said first group and the third subset of said second group to apply a first boosting voltage (see fig. 6), a second plurality of word lines coupled to the second subset of the first group and the fourth subset of the second group (see fig. 6) to apply a second boosting voltage; the at least one bounding word line being part of said first plurality of word lines or being part of the second plurality of word lines (see fig. 6); the voltage potential of the channel being a capacitively coupled voltage potential resulting from the first boosting voltage and the second boosting voltage (see col. 5, lines 7-10 and lines 25-28).

Regarding claims 39 and 43, Lutze et al. further disclose a plurality of bit lines including a first bit line coupled to said first group and a second bit line coupled to the second group, the first bit line applying a program inhibit voltage to the first group and the second bit line applying a program inhibit voltage to the second group while the second plurality of word lines applying the second boosting voltage (see figs. 6 and 16); the at least one bounding word line including a first bounding word line on a source side of the non-volatile storage element to be inhibited and a second bounding word line on a drain side of the non-volatile storage element to be inhibited (see figs. 6 and 16).

Regarding claims 44-47, Lutze et al. disclose the first group of non-volatile storage elements being a first string of NAND flash memory devices, the second group of

non-volatile storage elements being a second string of NAND flash memory devices (see fig. 6 and col. 5, lines 35-42); the first group and said second group of non-volatile storage elements being groups of multi-state flash memory devices (see fig. 12); the first group and the second group being part of an array of non-volatile storage elements (see fig. 6); the array being in communication with a host system; the array being removable from said host system or embedded in the host system (see col. 6, line 65 to line 12 of col. 7).

Regarding claims 49-51, Lutze et al. disclose in figs. 6 and 14-18, the means for programming boosts a voltage potential of said channel of the first means by applying a first boosting voltage to the first subset of the first group and a second boosting voltage to the second subset of the first group (see fig. 16), wherein the means for programming traps at least a portion of the voltage potential by lowering the first boosting voltage on at least one word line bounding the first subset of the first means subsequent to boosting the voltage potential, the at least one word line being coupled to a non-volatile storage element of the first subset of the first means (see figs 6 and 16), wherein the means for programming traps at least a portion of the voltage potential by lowering the second boosting voltage on at least one word line bounding the first subset of the first means subsequent to boosting the voltage potential, the at least one word line coupled to a non-volatile storage element of said second subset of the first means (see figs. 6 and 16).

Regarding claims 52-55, the apparatus as described above would perform the method as recited in claims 52-55.

Allowable Subject Matter

7. Claims 4-7, 9-10, 17, 19-21, 38 and 40-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or suggest a method of programming non-volatile memory comprising lowering a second boosting voltage for a first portion of a second subset and then lowering a second boosting voltage for a second portion of a second subset as recited in claims 4 and 14; first boosting voltage being lower than said second boosting voltage as recited in claim 5; the step of boosting including applying a first boosting voltage to a third subset of the second group of non-volatile storage elements and applying a second boosting voltage to a fourth subset of the second group of non-volatile storage elements as recited in claim 9; the step of boosting including applying a first boosting voltage to said first subset of said first group and said third subset of said second group and applying a second boosting voltage to said second subset of said first group and said fourth subset of said second group as recited in claims 19-21. Further, the prior art does not teach or suggest said voltage potential of said channel being higher than an isolated voltage potential of said portion of said channel associated with said first subset resulting from applying said first boosting voltage and lower than an isolated voltage potential of a portion of said channel associated with said second subset resulting from applying said second boosting voltage as recited in claim 38; the second bit line having a program enable voltage applied thereon subsequent to said second plurality of word lines having said second boosting voltage lowered thereon as recited in claim 40.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen et al. (U.S. 2004/0145024 A1) disclose a NAND string memory array providing boosting of a half-selected memory cell channel.

Hemink (U.S. 2005/0174852 A1) disclose a self-boosting system for flash memory cells.

Nazarian (U.S. 6,977,842) discloses a boosted substrate/tub programming for flash memories.

Choi et al. (U.S. 6,469,933) disclose a method for programming a non-volatile memory device.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Le whose telephone number is (571) 272-1872. The examiner can normally be reached on M-F (8.00AM - 5.30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL
February 01, 2006

2/6/06

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